and analysis—it would be helpful if the Examiner would read the specifications in conjunction with examining in detail the drawings—accordingly, the attention of the Examiner is directed to the drawings, 1A through 1I all of which show portions of the TiN layer still present—how can the Examiner say or honestly believe that the Admitted Prior Art shows the "removing the first layer of photoresist and the layer TiN.] depositing a blanket layer (114), forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

I t should be perfectly clear that this rejection is overcome because the Admitted Prior Art does not anticipate the present invention because the Admitted Prior Art does not remove the remaining portions of the layer of TiN after the remaining portions of the first layer of photoresist is removed. Applicants therefore submit that the Application is allowable and request an early allowance. In addition, because the Examiner did not find any other art that either anticipated or disclosed, taught or suggested the method as taught and claimed in the present application.

The Examiner rejected Claims 1 – 5 under 35 U.S.C. §103(a) as being unpatentable over the Admitted Prior Art. The Examiner stated:

> Referring to figures 1a-1I, the Admitted Prior Art teaches a method of manufacturing a semiconductor device comprises: forming a final metal layer (104) over the interlayer dielectric (102), forming a TiN layer (106) over the metal layer, forming a layer of photoresist (108) over the TiN layer, etching in the layer of TiN and the final layer of metal exposing portions of the interlay dielectric layer (sic), removing the first layer of photoresist and the layer TiN **[again it would be helpful for the Examiner to be accurate in his comments and analysis—the layer of TiN is not removed when the layer of photoresist is removed—this is what causes the problems in the industry, i.e., what was being sought in the industry was a manufacturing process that does not require the step of etching the TiN layer during pad etch]**, depositing a blanket layer (114) , forming a second photoresist layer (116) on the blanket layer of interlayer dielectric; patterning and developing the second layer of the photoresist layer exposing portions of blanket layer interlayer dielectric overlying metal structures; and etching the exposed portion of the blanket layer of interlayer dielectric down to the metal structures, removing the second layer of the photoresist (see figures 1a-1I of the Admitted Prior art and related text).

The Examiner admitted:

> However, the reference does not teach etching the photoresist layer and TiN layer by using fluorine containing gas chemistry at an elevated temperature.

The Examiner further stated:

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The examiner takes Official Notice that the embodiment described in claim 5 would have been obvious to skilled worker in the art at the time the invention was made because determining an optimum material for etching the layer only involved routine skill in the art (see MPEP 2144.03).

This rejection is overcome because the Examiner has completely misread the specification and the drawings. The layer of TiN is not removed when the first layer of photoresist is removed and before the second layer of interlayer dielectric is formed. **Note the structure (106) throughout the drawings, 1A – 1H, and note that a small portion of the TiN remains in figure 1I.**

Because the Admitted Prior Art, contrary to what the Examiner has stated, does not anticipate the claims and further, because the Admitted Prior Art does not disclose, teach or suggest the method as disclose and claimed in the present application, Applicants submit that the application is allowable and request an early allowance.

Respectfully submitted,

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I certify that this document is being deposited on 7/3/00 with the U.S. Postal Service as first class mail under 37 C.F.R. §1.8 addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

H. D. Nelson
Signature

H. D. NELSON
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